METHOD AND SYSTEM FOR LOGIC VERIFICATION USING MIRROR INTERFACE

ABSTRACT OF THE DISCLOSURE

Verification of external interfaces of cores on system-on-chip (SOC) designs frequently entails the purchase of costly standardized software models to test the external interfaces. Typically, the standardized models provide more functionality than is needed. Instead of standardized models, test models may be developed and utilized, but this also incurs cost and delay. The present invention provides an efficient and economical alternative. A mirror interface, or copy of the external interface undergoing verification, is used with a standardized control mechanism to verify the external interface. Because all interface I/O connections can thereby be utilized, a cost-effective and highly reusable way of verifying such interfaces is provided.